Ref No:

Sri Krishna Institute of Technology, Bengaluru-560090

COURSE PLAN

Academic Year - 2019-2020

Academic Evaluation and Monitoring Cell

Program:	BE- Electrical and Electronics Engineering
Semester:	3
Course Code:	18EEL38
Course Title:	Electronics Laboratory
Credit/L-T-P:	2 / 0-2-2
Total Contact Hours:	40
Course Plan Author:	Avinash S

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Table of Contents

INSTRUCTIONS TO TEACHERS

- Classroom / Lab activity shall be started after taking attendance.
- Attendance shall only be signed in the classroom by students.
- Three hours attendance should be given to each Lab.
- Use only Blue or Black Pen to fill the attendance.
- Attendance shall be updated on-line & status discussed in DUGC.
- No attendance should be added to late comers.
- Modification of any attendance, over writings, etc is strictly prohibited.
- Updated register is to be brought to every academic review meeting as per the COE.

Note : Remove “Table of Content” before including in CP Book

18EEL38 : ELECTRONICS LABORATORY

A. LABORATORY INFORMATION

1. Lab Overview

Degree:	B.Tech	*Program:*	EE
Year / Semester :	2 / 3	*Academic Year:*	2019
Course Title:	Electronics Laboratory	*Course Code:*	18EEL38
Credit / L-T-P:	2 / 0-2-2	*SEE Duration:*	180 Minutes
Total Contact Hours:	40Hrs	*SEE Marks:*	60 Marks
CIA Marks:	40	*Assignment*	1 / Module
Course Plan Author:	Mr. Avinash S	*Sign*	Dt :
Checked By:		*Sign*	Dt :

2. Lab Content

Unit	Title of the Experiments	Lab Hours	Concept	Blooms Level
1	Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits withand without Capacitor filter. Determination of ripple factor, regulation and efficiency.	3	Rectification	L5
2	Static Transistor characteristics for CE, CB and CC modes and determination of h parameters.	3	Characteristics	L3
3	Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.	3	Frequency Response	L4
4	Design and testing of BJT - RC phase shift oscillator for given frequency of oscillation.	3	Signal Generation	L5
5	Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping	3	Small signal analyses of Darlington emitter follower	L3
6	Simplification, realization of Boolean expressions using logic gates/Universal gates.	3	Realization	L3
7	Realization of half/Full adder and Half/Full Sub tractors using logic gates	3	Realization	L3
8	Realization of parallel adder/Sub tractors using 7483 chip- BCD to Excess-3 code conversion and Vice - Versa.	3	Realization	L3
9	Realization of Binary to Gray code conversion and vice versa	3	Realization	L3
10	Design and testing Ring counter/Johnson counter	3	Counter Design	L5
11	Design and testing of Sequence generator	3	Sequence generator	L5
12	Realization of 3 bit counters as a sequential circuit and MOD – N counter design using 7476, 7490, 74192, 74193	3	MOD – N Counter Design	L5

3. Lab Material

Unit	Details	Available
1	Text books	

	Digital Logic Applications and Design by John M Yarbrough & Donald D Givone,Electronic Devices and CircuitTheory by Robert L Boylestad Louis Nashelsky & Electronic Devices and Circuits by David A Bell.	In Lib
2	Reference books	
	Logic and computer design Fundamentals by M. Morries Mano and Charles Kime, Fundamentals of logic design byCharles H Roth, JR and Larry L. Kinney, Fundamentals of Digital Circuits by A. Anand Kumar , A Text Book of Electrical Technology, Electronic Devices and Circuits by B.L. Theraja, A.K. Theraja, Electronic Devices and Circuits by Anil K. Maini VashaAgarval & Fundamentals of Analog Circuits by Thomas L Floyd.	In dept
3	Others (Web, Video, Simulation, Notes etc.)	
		Not Available

4. Lab Prerequisites:

-	-	Base Course:		-	-
SNo	Course Code	Course Name	Topic / Description	Sem	Remarks
1	17ELN24	Basic Electronics	1. Knowledge Digital Electronics Fundamentals	2	

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

5. General Instructions

SNo	Instructions	Remarks
1	Keep the lab neatly. Maintain silence.	
2	Maintain your lab observation and lab manual.	
3	Prepare your experiment in well advance.	
4	Check the power supply before use.	
5	Maintain discipline in the lab.	
6	After completion of your experiment switch off the power supply.	
7	Observation book and Lab record are compulsory.	
8	Students should report to the concerned lab as per the time table.	
9	After completion of the experiment, certification of the concerned staff in-charge in the observation book is necessary.	
10	Student should bring a notebook of 100 pages and should enter the readings /observations into the notebook while performing the experiment.	

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Students are expected to study the circuit, theory and procedures, expected output before doing the experiment.	
2	Adjustment of signal generator: - Before connecting the signal generator to the circuit check the followings. a. Set the shape of the waveform (sinusoidal), b. Set the frequency using coarse and fine adjustments. c. Set the offset adjustments. Set the CRO in DC mode and ensure the waveform is symmetry in both positive and negative cycle. If not , adjust it using the DC offsetting potentiometer d. Set the voltage magnitude using Vcourse settings and Vfine adjustments.	
3	Adjustment of CRO: a. Select the right voltage and time scale to get the proper waveform b. For clipper and clamper circuits, observe the waveform in DC mode only c. Set the input waveform mainly for offset setting in DC mode only. d. Before measurement, ensure X & Y are in calibrated mode (if provided externally) e. Ensure that Channel selection and trigger mode are properly set.	

	f. In case of two channels do not mix the signal and ground terminals	
4	Multi-meter adjustments:- a. Set the right mode before taking the readings. b. For current reading, connect the multimeter in mA (or A) mode to the circuit before switching on the supply. Do not remove the current meter when the supply is on. Check for ac and dc modes as required. c. For voltage reading ensure that proper ac or dc setting. d. Use the proper leads for the measurement. Wrong cables damage the instrument.	
5	After adjusting the input voltage, check the circuit connections before turning the power on.	
6	After adjusting the input voltage, check the circuit connections before turning the power on.	
7	Don't pull out the connections with the power supply on.	
8	Wear your College ID card Do not operate the IC trainer kits without permission	
9	Avoid loose connection and short circuits	
10	Do not interchange the ICs while doing the experiment	
11	Handle the trainer kit properly	
12	Do not panic if you do not get the output	
13	After completion of the experiment switch off the power and return the components	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
1	Design & Analyses of Full wave Rectifiers using hardware components	03	Rectification	Conduction	Test & Viva Voce	L5
2	Determine Characteristic of CE, CB & CC modes of h parameters using hardware components	03	Characteristics	Conduction	Test & Viva Voce	L3
3	Analyze the frequency response of BJT & FET using using hardware components	03	Frequency Response	Conduction	Test & Viva Voce	L4
4	Analyses & Design of BJT-RC phase shift of oscillator for given fequency using using hardware components	03	Signal Generation	Conduction	Test & Viva Voce	L5
5	Determine the gain, i/p & o/p of BJT using hardware components	03	Small signal analyses of Darlington emitter follower	Conduction	Test & Viva Voce	L3
6	Realize the Boolean expression with their truth table using LD trainer kit.	03	Realization	Conduction	Test & Viva Voce	L3
7	Realize the Adders & Substractors with their truth table using LD trainer kit.	03	Realization	Conduction	Test & Viva Voce	L3
8	Realize the parallel adder/Subtractors with their truth table using LD trainer kit.	03	Realization	Conduction	Test & Viva Voce	L3
9	Realize the Binary to Gray code & vice versa using LD trainer kit.	03	Realization	Conduction	Test & Viva Voce	L3
10	Design & Realize the Ring & Jogn counter using LD trainer kit.	03	Counter Design	Conduction	Test & Viva Voce	L5
11	Design & Realize the Sequence generator using LD trainer kit.	03	Sequence generator	Conduction	Test & Viva Voce	L5
12	Design & Realize the MOD – N Counter Design using LD trainer kit.	03	MOD – N Counter Design	Conduction	Test & Viva Voce	L5
-	**Total**	**36**	-	-	-	-

Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

2. Lab Applications

SNo	Application Area	CO	Level
1	The full wave rectifier circuit is one that is **widely** used for power supplies and many other areas where a full wave rectification is required. The full wave rectifier circuit is used in most rectifier applications because of the advantages it offers.	CO1	L5
2	CE - common emitter : most commonly used in general purpose amplifier designs. It provides high gain and high input impedance. The drawbacks with this simple configuration are limited bandwidth due to Miller effect of collector-base capacitance and limited load driving capability due to high output impedance. CE is also used in digital (large signal) designs as switching stage. CC - common collector : commonly used as unity gain buffer and sometimes called emitter follower. It provides high input impedance, low output impedance and high bandwidth. Perfect for driving heavy loads. The drawback is no gain; gain is close to but less than one. Therefore, it is typically used in conjunction with an amplifier and not instead of an amplifier. CC is also used as a voltage translation stage. CB - common base : commonly used as a cascode stage to isolate output voltage signal from feeding back to input eliminating Miller effect from amplifier to increase bandwidth. It provide low input impedance and close to unity current gain. It is not typically used as a standalone amplifier due to low input impedance. CB is also used to increase output impedance of current sources to increase gain.	CO2	L3
3	FETs are widely used as input **amplifiers** in oscilloscopes, electronic voltmeters and other measuring and testing equipment because of their high input impedance	CO3	L4
4	RC Phase Shift Oscillators are used in musical instruments, voice synthesis and in GPS units since they work at all audio frequencies.	CO4	L5
5	The bipolar junction transistor (BJT) is used in logic circuits. The BJT is used as an oscillator. It is used as an amplifier.	CO5	L3
6	Used to simplify the expressions.	CO6	L3
7	Adders & Subtractors are wildly used in in computer's ALU (Arithmetic logic unit) to compute addition as well as CPU (Central Processing unit) and GPU (Graphics Processing unit) for graphics applications to reduce the circuitcomplexity. Adder and subtractor are basically used for performing arithmetical functions like addition, subtraction, multiplication and division in electronic calculators and digital instruments. Adders are used in digital calculators for arithmetic addition and devises that uses some kind of increment or arithmetic process They are also used in microcontrollers for arithmetic additions, PC (program counter) and timers.	CO7	L3
8	Parallel adder is basically used in binary digit bit to add multiple n - bits in it. So mean while it act like auxiliary full adder. While, parallel subtractor is deduction of n-bits form binary digit.	CO8	L3
9	Gray code has property that **two successive numbers differ in only one bit** because of this property gray code does the cycling through various states with minimal effort and used in K-maps, error correction, communication etc.	CO9	L3
10	Used for decimal arithmetic in computers and calculators.	CO10	L5
11	The sequence generator is used to generate primary key values & it's used to generate numeric sequence values like 1, 2, 3, 4, 5 etc	CO11	L5
12	The main application of counter is to count events , and each event is converted in to one clock cycle. That means counter is used to count number of clocks.	CO12	L5

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes	

#	COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	Level
18EEL38.1	Design & Analyses of Full wave Rectifiers using hardware components	2.71	2.71	3								2.92		L5
18EEL38.2	Determine Characteristic of CE, CB & CC modes of h parameters using hardware components	2.71	2.71											L3
18EEL38.3	Analyze the frequency response of BJT & FET using using hardware components	2.71	2.71									2.92		L4
18EEL38.4	Analyses & Design of BJT-RC phase shift of oscillator for given fequency using using hardware components	2.71	2.71	3								2.92		L5
18EEL38.5	Determine the gain, i/p & o/p of BJT using hardware components	2.71	2.71											L3
18EEL38.6	Realize the Boolean expression with their truth table using LD trainer kit.	2.71	2.71											L3
18EEL38.7	Realize the Adders & Substractors with their truth table using LD trainer kit.	2.71	2.71											L3
18EEL38.8	Realize the parallel adder/Subtractors and BCD to Excess-3 code conversion with their truth table using LD trainer kit.	2.71	2.71											L3
18EEL38.9	Realize the Binary to Gray code & vice versa using LD trainer kit.	2.71	2.71											L3
18EEL38.10	Design & Realize the Ring & Jogn counter using LD trainer kit.	2.71	2.71	x								2.92		L5
18EEL38.11	Design & Realize the Sequence generator using LD trainer kit.	2.71	2.71	3								2.92		L5
18EEL38.12	Design & Realize the MOD – N Counter Design using LD trainer kit.	2.71	2.71	3								2.92		L5
18EEL38.	Average													

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Mapping		Mapping Level	Justification
CO	**PO**	**-**	**-**
CO1	PO1	L1	
CO1	PO2	L3	
CO1	PO5		

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teaching Hours	No. of question in Exam							CO	Levels
			CIA-1	CIA-2	CIA-3	Asg-1	Asg-2	Asg-3	SEE		
1	Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits withand without Capacitor filter. Determination of ripple factor, regulation and efficiency.	03	1	-	-	-	-	-	1	CO1	L5
2	Static Transistor characteristics for CE, CB and CC modes and determination of h parameters.	03	1	-	-	-	-	-	1	CO2	L3
3	Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.	03	1	-	-	-	-	-	1	CO3	L4
4	Design and testing of BJT - RC phase shift oscillator for given frequency of oscillation.	03	1	-	-	-	-	-	1	CO4	L5
5	Determination of gain, input and output impedance of BJT - Darlington emitter follower with and without bootstrapping	03	1	-	-	-	-	-	1	CO5	L3
6	Simplification, realization of Boolean expressions using logic gates/Universal gates.	03	1	-	-	-	-	-	1	CO6	L3
7	Realization of half/Full adder and Half/Full Subtractors using logic gates	03	1	-	-	-	-	-	1	CO7	L3
8	Realization of parallel adder/Sub tractors using 7483 chip- BCD to Excess-3 code conversion and Vice - Versa.	03	1	-	-	-	-	-	1	CO8	L3
9	Realization of Binary to Gray code conversion and vice versa	03	1	-	-	-	-	-	1	CO9	L3
10	Design and testing Ring counter/Johnson counter	03	-	1	-	-	-	-	1	CO10	L5
11	Design and testing of Sequence generator	03	-	1	-	-	-	-	1	CO11	L5
12	Realization of 3 bit counters as a sequential circuit and MOD – N counter design using 7476, 7490, 74192, 74193	03	-	1	-	-	-	-	1	CO12	L5
-	**Total**	**36**								-	-

Note: Write CO based on the theory course.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	30	CO1, CO2, CO3, CO4	L23, L3
CIA Exam – 2	30	CO5, CO6, CO7,	L1, L2, L3 . .
CIA Exam – 3	30	CO8, CO9	L1, L2, L3 . .
Assignment - 1	05	CO1, CO2, CO3, CO4	L2, L3, L4 ...
Assignment - 2	05	CO5, CO6, CO7, CO8, CO9	L1, L2, L3 ...
Assignment - 3	05	CO8, CO9	L1, L2, L3 ...
Seminar - 1	05	CO1, CO2, CO3, CO4	L2, L3, L4 . ..
Seminar - 2	05	CO5, CO6,CO7,CO8, CO9	L2, L3, L4 . ..
Seminar - 3	05	CO8, CO9	L2, L3, L4 . ..
Other Activities – define – Slip test		CO1 to Co9	L2, L3, L4 . ..

Final CIA Marks	**40**	**-**	**-**

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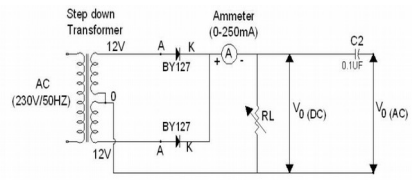
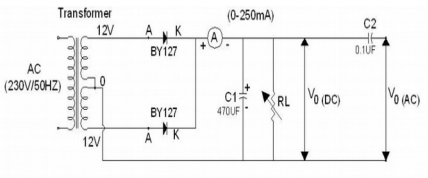
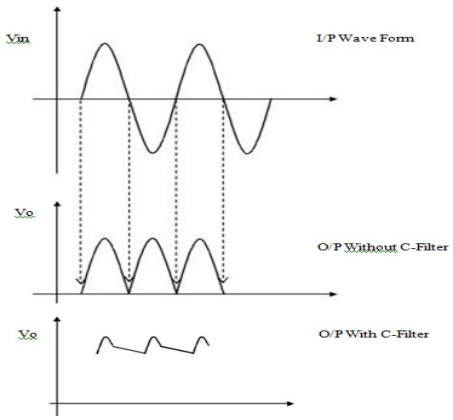
SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	05 Marks
2	Record Writing	10 Marks for each Expt
3	Internal Exam Assessment	25 Marks
4	Internal Assessment	40 Marks
5	SEE	60 Marks
-	**Total**	**100 Marks**

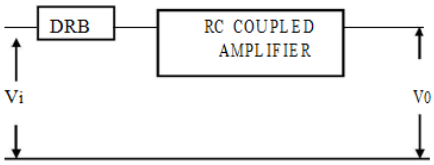
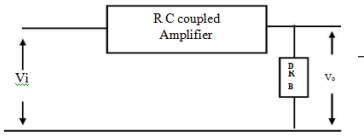
D. EXPERIMENTS

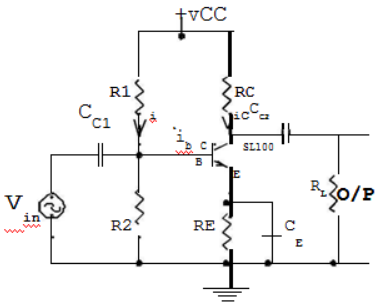
Experiment 01 : Structure of C program

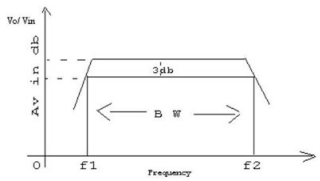
#	Experiment No.:	1	Marks		Date Planned		Date Conducted	
1	Title	**Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency.**						
2	Course Outcomes	Design & Analyses of Full wave Rectifiers using hardware components						
3	Aim	Design and testing of Full wave and bridge type rectifier circuits with and without capacitor and to determine ripple factor, regulation and efficiency						
4	Material / Equipment Required	Lab Manual/ CRO, Signal generator, capacitor, diodes, power chord, ameter, multi-meter, stepdown transformer.						
5	Theory, Formula, Principle, Concept	The conversion of AC into pulsating DC is called Rectification. Electronic Devices can convert AC power into DC power with high efficiency. The full-wave rectifier consists of a center-tapped transformer, which results in equal voltages above and below the center-tap. During the positive half cycle, a positive voltage appears at the anode of D1 while a negative voltage appears at the anode of D2. Due to this diode D1 is forward biased. It results a current Id1 through the load R. During the negative half cycle, a positive voltage appears at the anode of D2 and hence it is forward biased, resulting a current Id2 through the load. At the same instant a negative voltage appears at the anode of D1, reverse biasing it and hence it doesn't conduct.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	step 1: Rig up the circuit as per the circuit diagram shown.(without filter) step 2:Switch ON the multimeter in DC mode & Switch ON the Power supply and measure Vdc and Idc step 3: Now switch OFF the power supply & switch the multimeter in AC mode and switch ON the power supply to measure Vac and Iac. Calculate efficiency and Ripplefactor step 4:Rig up the circuit as per the circuit diagram shown.(with filter) step 5:Switch on the Power Supply and switch the multimeter in DC mode to measure Vdc and Idc step 6:Now switch the multimeter in AC mode and measure Iac step 7:Measure Vr(p-p) from CRO and calculate Vrms, efficiency and Ripplefactor.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 						
8	Observation Table, Look-up Table, Output	**Without Filter** SINO | RL Ω | I_{odc} ma | V_{odc} volts | V_{inrms} volts | V_{oac} volts | I_{oac} ma | RIPPLE γ | EFFICIENCY η | REGULATION **With Filter** SINO | RL Ω | I_{odc} ma | V_{odc} volts | V_{inrms} volts | V_{oac} volts | I_{oac} ma | RIPPLE γ | EFFICIENCY η | REGULATION						
9	Sample Calculations	**Without filter: Let Vinrms = 12V** Vodc = 2Vm/π = 10.8v = 10v Iodc = 100mA						

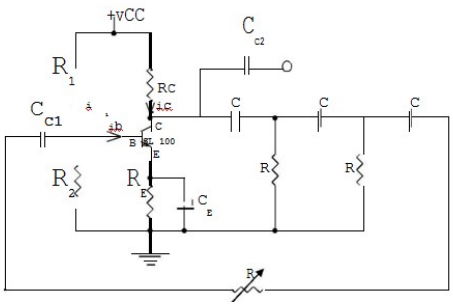
		RL (min) = Vodc/Iodc = 100Ω Let Rf = 10Ω Iorms = $\sqrt{Ioac^2+Iodc^2}$ **With filter:**Let Ripple = γ = Vorms /Vodc = 0.48 Let γ=6%=0.06, F = 50HZ and RL = 100 Ω WKT γ= $1/4\sqrt{3}$ F C RL C = 470mF **Ripple factor** = Voac/Vodc %**Efficiency** = $Iodc^2RL/Iorms^2$ (Rf+RL) %**Regulation** = (VNL-VFL)/VFL •
10	Graphs, Outputs	
11	Results & Analysis	Calculated the ripple factor, regulation and efficiency of Rectifiers (with and witout capacitors)
12	Application Areas	The full wave rectifier circuit is one that is **widely** used for power supplies and many other areas where a full wave rectification is required. The full wave rectifier circuit is used in most rectifier applications because of the advantages it offers.
13	Remarks	
14	Faculty Signature with Date	

Experiment 02 : Keywords and identifiers

-	**Experiment No.:**	3	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	**Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.**						
2	Course Outcomes	Analyze the frequency response of BJT & FET using using hardware components						
3	Aim	To design a RC-coupled Single Stage BJT amplifier and determine it's Gain-Frequency response input Impedance and output impendence						
4	Material/Equipment Required	Lab Manual/ CRO, Signal generator, capacitor, diodes, power chord, ameter, multi-meter.						
5	Theory, Formula, Principle, Concept	This is most popular type of coupling as it provides excellent audio fidelity. A coupling capacitor is used to connect output of first stage to input of second stage. Resistances R1, R2, Re form biasing and stabilization network. Emitter bypass capacitor offers low reactance paths to signal coupling Capacitor transmits ac signal, blocks DC. Cascade stages amplify signal and overall gain is increased total gain is less than product of gains of individual stages. Thus for more gain coupling is done and overall gain of two stages equals to A = A1*A2 A1 = voltage gain of first stage, A2 = voltage gain of second stage. When ac signal is applied to the base of the transistor, its amplified output appears across the collector resistor Rc. It is given to the second stage for further amplification and signal appears with more strength. Frequency response curve is obtained by plotting a graph between frequency and gain in db .The gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. The gain decreases in the low frequency range due to coupling capacitor Cc and at high frequencies due to junction capacitance Cbe.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	a)**To plot Frequency response:** 1.Rig up the circuit as per the given circuit diagram. 2.Switch on the D.C. power supply and check the D.C. conditions without any input signal and record in table 1. 3.Select sine waves input and set the input signal frequency at 10 KHz constant and observe the input wave and output wave on the CRO and adjust the input amplitude such that the output is undistorted waveform. Calculate mid-band gain using AV = V0 (p-p) / Vin (p-p). 4.Keeping the input amplitude constant, vary the frequency from 50hz to 1Mhz and note down the corresponding output voltage (p-p) in the table 2. 5.Calculate gain in db and plot the frequency response curve and find the bandwidth. b)To find input impedance Zin:  1.Connect DRB in series with the input signal and set it to ZERO. 2.Set the signal frequency to 10 kHz and measure the output Vo (p-p). 3.Vary the DRB from 0 to Zin such that the output signal voltage reduces to half its value. This value of DRB at which the output signal reduces to half its initial value is the input Impedance Zin. c)To find output impedance Zo:  						

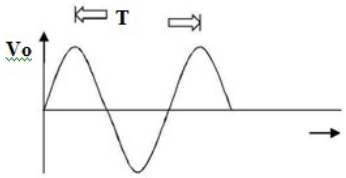
		1.Connect DRB in parallel with the output and set it to MAXIMUM. 2.Set the signal frequency to 10 KHz and measure the output Vo (p-p). 3.Vary the DRB from maximum to minimum such that the output signal voltage reduces to half its value, this value of DRB at which the output signal reduces to half its value is the output impedance Zo.
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	
8	Observation Table, Look-up Table, Output	Table 1: D.C. Conditions: Parameter | V_{RC} | V_{CE} | V_{RE} | V_{BE} | VB Theoretical | 4.8 | 6 | 1.2 | 0.7 | 1.9 Practical | | | | | Table 2: Frequency response Vin =..... Volts F hz | Vo (p-p) | AV = Vo (p-p) / Vin (p-p). | AV in db = 20*log AV 50 | | | ..... | | | ..... | | | ..... | | | ..... | | | ..... | | | 1 MHz | | |
9	Sample Calculations	**DESIGN:** Let VCC=12V; IC=4.5mA; β=100(SL100); VCE=12/6=6v **To find RE**:Let VRE= VCC/10 =12/10=1.2v i.e., IERE = 1.2v Therefore RE= VRE / IE=1.2 / 4.5mA= 267Ω=270Ω(standard value) **To find RC**:From the Collector-Emitter loop writing KVL we get VCC- ICRC - VCE –VRE = 0 \ RC = (VCC – VCE – VRE) / IC (12-6-1.2)/4.5mA= 1.07KΩ (1KΩ std) **To find R1 and R2:** From the above biasing circuit VB= VBE + VRE = 0.7 + 1 = 1.7v IC = βIB Or IB = IC / β = 4.5mA/100 = 0.04mA Assuming 10IB flowing in R1 and 9IB flowing in R2

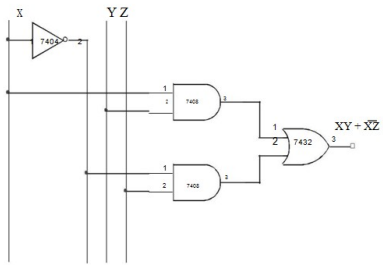
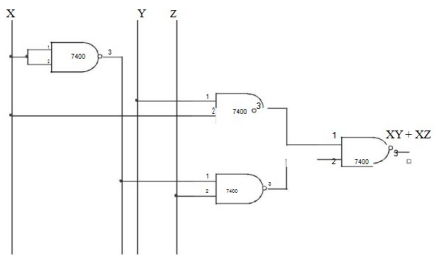
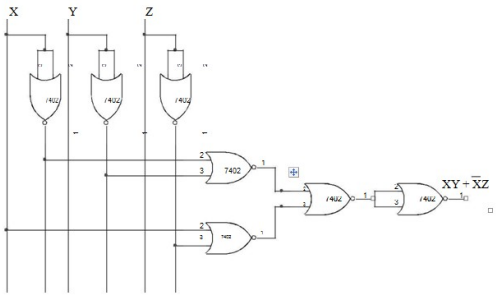
		Now R1 = (VCC – VB) /I1 = (VCC- VB)/10IB R1 = 22.4 KW. **R1 = 22 K**W (standard value) Assume only IB out of 10IB flows through base, therefore remaining 9IB of current flows through R2. Therefore R2 = VB / (I1-IB) = VB/9IB R2 = 4.69KW **R2 = 4.7 K**W (standard) **To find By-Pass Capacitor CE and Coupling Capacitor CC1 and CC2** Bipass Capacitor is selected by taking lower cutoff frequency f=100Hz Let XCE = (1/10) RE at f = 100 HZ i.e. (1/2πfCE) = RE / 10 \CE = (10/2π*100*270) = 59µF **CE = 47 µF** (Standard Value)
		Also use **CC1= CC2 = 0.47 µF** (Ceramic) **Input Impedance (Zin):** In order to calculate the input impedance first calculate the value of Zin (base) = β re, where re is the resistance of the emitter diode re @ 25 mV / IC = 25mV / 4.5mA = 5.56W Zin (base) = β re = 100 * 5.56 = 555.556W The input impedance of an amplifier is the input impedance seen by the a.c source driving the amplifier. Therefore the biasing resistor R1 and R2 are included as follows Zin = Zin (base) + (R1 || R2) Zin = 4.43KW **Output impedance (Z0):** The output impedance is given by Z0 = RC || RL Let RL = 1 KW. \ **Z0 = 516.908** W **Voltage Gain AV:** Voltage gain is given by AV = (RC || RL)/ re = 516.908/5.56 **AV= 92.96**
10	Graphs, Outputs	
11	Results & Analysis	Determined the half power points, bandwidth, input and output impedances.
12	Application Areas	Audio Amplifiers.
13	Remarks	
14	Faculty Signature with Date	

#	Experiment No.:	4	Marks		Date Planned		Date Conducted	
1	Title	**DESIGN AND TESTING OF BJT - RC PHASE SHIFT OSCILLATOR FOR GIVEN FREQUENCY OF OSCILLATION**						
2	Course Outcomes	Analyses & Design of BJT-RC phase shift of oscillator for given fequency using using hardware components						
3	Aim	design and test a RC-phase shift oscillator for a frequency of 10 kHz						
4	Material / Equipment Required	Lab Manual/ CRO, Signal generator, capacitor, resistors, power chord, ammeter, multi-meter, BJT.						
5	Theory, Formula, Principle, Concept	RC phase shift oscillator consists of a single transistor amplifer and a RC phase shift network. The Phase shift network consists of three RC sections. Here a fraction of the output of the amplifier passed through a phase shift network before feeding back to the input. The phase shift in each section is 600 so that the total phase shift is 1800. Another 1800 phase shift is provided by the transistor amplifier and there the total phase shift of the oscillator is 3600. The frequency of oscillation is given by fo = 1/[2π√6(RC)]. Let us consider a RC circuit. Let I be the current flowing through R and C. Then using I as the reference vector, Vo is in phase with I while Vc, the voltage across the capacitor 900 behind as shown in the figure. Vi is the sum of Vo and Vc. Hence Vc is θ degrees ahead of Vi and represents a phase shift of θ degrees. Vo=IR, Vc=IXc Tan θπfCR) Therefore f = 1/(2πfCRTan θ)						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Rig up the circuit as shown in the diagram. 2.Switch on the D.C. power supply and measure the D.C. conditions and record in table 1 3.Obtain the output waveform on the CRO and measure the period of oscillation and the amplitude. Calculate the frequency and compare with theoretical value.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output	Table 1: D.C. Conditions:						

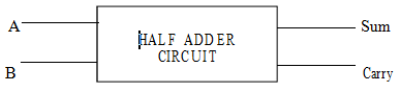
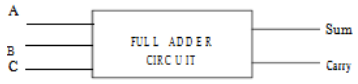
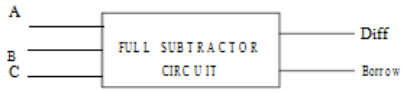
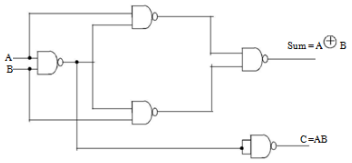
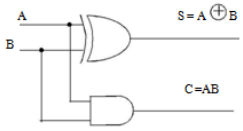
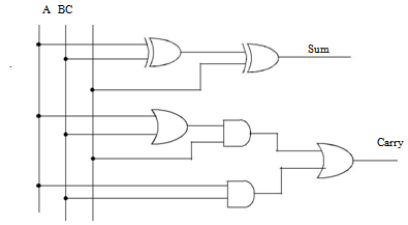
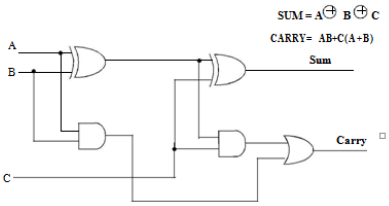
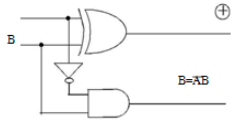
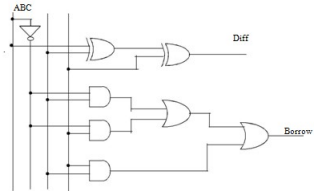
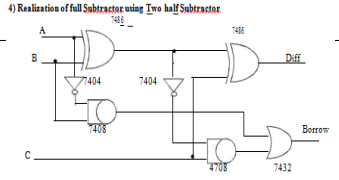
Parameter	V_{RC}	V_{CE}	V_E	V_{BE}	V_B
Theoretical	4.8	6	1.2	0.7	1.9
Practical					

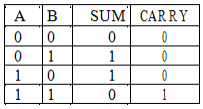
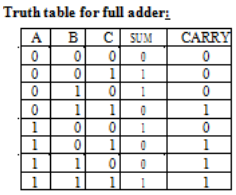
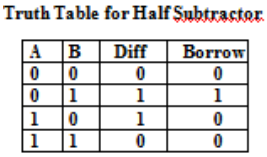
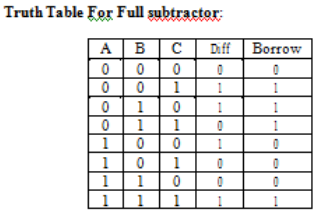
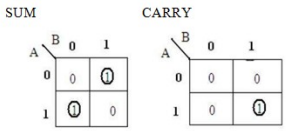
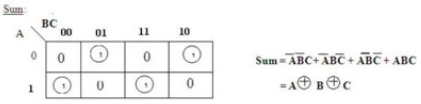
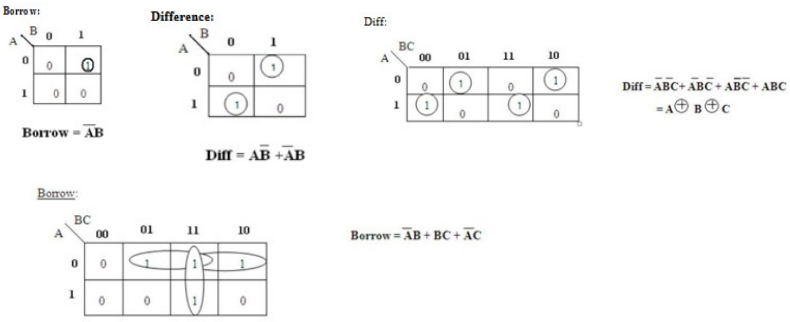
9	Sample Calculations	**DESIGN:** Let V_{cc} = 12V; I_C = 4.5mA; β = 100 (SL100); V_{CE} = 12/2=6V **To find R_E** Let $V_{RE} = V_{CC}/10$= 12/10=1.2						

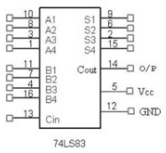
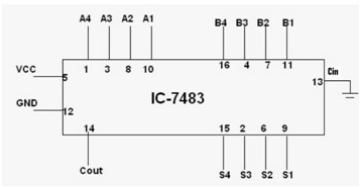
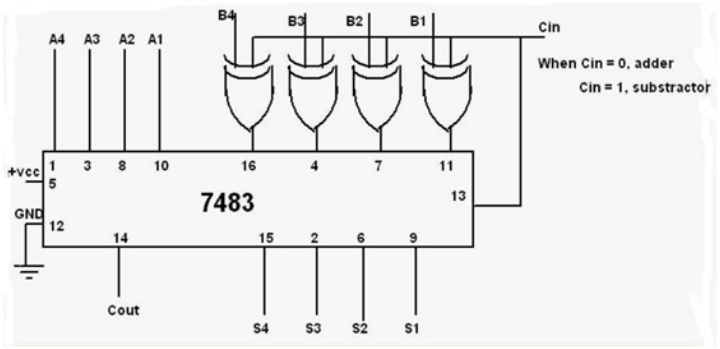
		Therefore RE = VRE/IE ≈ VRE/IC = 1.2/4.5Ma =267Ω (270 Ω std) **To find RC** From the Collector-Emitter loop writing KVL we getVCC- ICRC - VCE –VRE = 0 \ RC = (VCC – VCE – VRE) / IC =(12-6-1.2)/4.5mA=1.07KW (1KW std)
10	Graphs, Outputs	
11	Results & Analysis	for (Theoritical) = 2kHz. for (practical) = ----- kHz.
12	Application Areas	
13	Remarks	
14	Faculty Signature with Date	

#	Experiment No.:	6	Marks		Date Planned		Date Conducted	
1	Title	**SIMPLIFICATION, REALIZATION OF BOOLEAN EXPRESSIONS USING LOGIC GATES /UNIVERSAL GATES.**						
2	Course Outcomes	Design & Analyses of Full wave Rectifiers using hardware componentsRealize the Boolean expression with their truth table using LD trainer kit.						
3	Aim	To Simplify and realize given Boolean expressions using basic gates & Universal Gates.						
4	Material / Equipment Required	Lab Manual/ Trainer kit, power chord, patch chords, IC's						
5	Theory, Formula, Principle, Concept	**Expressions:** 1) $A = XY + \overline{X}Z + YZ$ 2) $Y = ABC + ABC + ABC + ABC$ 3) $Y = (A+B+C)(A+B+C)(A+B+C)$						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Identify the IC required and Place the IC in the socket of the trainer kit. 2.Make the connections as shown in the circuit diagram. 3.Apply the different combinations of input according to truth table and verify the output.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	1) Realization Using Basic Gates  2) Realization Using Universal (Nand) Gates  3) Realization Using Nor Gates  						
8	Observation Table, Look-up Table, Output							
9	Sample Calculations	$A = XY + \overline{X}Z + YZ = XY + \overline{X}Z + YZ(X+\overline{X}) = XY + \overline{X}Z + XYZ + \overline{X}YZ$ $= XY(1+Z) + \overline{X}Z(1+Y)$ $A = XY + \overline{X}Z$						
10	Graphs, Outputs	-						
11	Results & Analysis	Realization of Boolean Expressions using truth table						
12	Application Areas							
13	Remarks							
14	Faculty Signature with Date							

X	Y	Z	XY	$\overline{X}Z$	A =XY +$\overline{X}$Z
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	1	0	1
1	1	1	1	0	1

#	Experiment No.:	7	Marks		Date Planned		Date Conducted	
1	Title	**REALIZATION OF HALF/ FULL ADDER AND HALF/ FULL SUBTRACTOR USING LOGIC GATES /UNIVERSAL GATES**						
2	Course Outcomes	Realize the Adders & Substractors with their truth table using LD trainer kit.						
3	Aim	To realize half/ full adder and substractor using logic gates /universal gates.						
4	Material / Equipment Required	Lab Manual/ Trainer kit, power chord, patch chords, IC's						
5	Theory, Formula, Principle, Concept	  Half Adder and Full Adder Circuit. An adder is a digital circuit that performs addition of numbers. The half adder adds two binary digits called as augend and addend and produces two outputs as sum and carry; XOR is applied to both inputs to produce sum and AND gate is applied to both inputs to produce carry.   The full subtractor is a combinational circuit which is used to perform subtraction of three input bits: the minuend , subtrahend , and borrow in . The fullsubtractor generates two output bits: the difference and borrow out.							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Identify the IC required and Place the IC in the socket of the trainer kit. 2.Make the connections as shown in the circuit diagram. 3.Apply the different combinations of input according to truth table and verify the output.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	Circuit diagram: 1) Realization of half adder using only NAND gates  2) Realization of half adder using Ex-clusive OR and basic gates  3) Realization of full adder using Ex-clusive OR and basic gates  4) Realization of full adder using Two half adder's  2) Realization of half subtractor using Ex-clusive OR and basic gates  3) Realization of full subtractor using Ex-clusive OR and basic gates  4) Realization of full Subtractor using Two half Subtractor 							

8	Observation Table, Look-up Table, Output	   
9	Sample Calculations	  
10	Graphs, Outputs	
11	Results & Analysis	
12	Application Areas	
13	Remarks	
14	Faculty Signature with Date	

#	Experiment No.:	8	Marks		Date Planned		Date Conducted	
1	Title	Realization of parallel adder/Sub tractors using 7483 chip- BCD to Excess-3 code conversion and Vice - Versa.						
2	Course Outcomes	Realize the parallel adder/Sub tractors and BCD to Excess-3 code conversion with their truth table using LD trainer kit.						
3	Aim	To Realize a) Parallel Adder / subtractor using 7483. b) BCD to EXCESS – 3 code conversion and vice versa using 7483						
4	Material / Equipment Required	Lab Manual/ Trainer kit, power chord, patch chords, IC's						
5	Theory, Formula, Principle, Concept	IC PIN FUNCTION DIAGRAM:  74LS83 4 –Bit binary adder:  **BCD To EXCESS – 3 Code conversion and vice versa** **NOTE:** BCD + 0011 = EX-3 Keep C_{in} = 0 EX-3 – 0011 = BCD Keep C_{in} = 1						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Make the connections as shown in the fig 2.For Addition make Cin=0 and apply 4 bits of i/p for A and apply another set of 4 bit to B. Observe the O/P at S3 S2 S1 S0 and Carry generated at Cout. Repeat the steps for different inputs and tabulate the results. 3.For Subtraction, Cin=1(A-B). By XOR-ing the i/p bits of B by 1, 1's complement of B is obtained. 4.Verify the the difference at S0,S1,S2,S3 and Cout. If Cout is 0, difference is _ve and difference is in 2's Complement form. If Cout is 1, difference is +ve. 5.Repeat the above steps for different inputs and tabulate the result.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	a)4-Bit Parallel adder/Substractor:  						
8	Observation Table, Look-up Table, Output	**1. To subtract a smaller Number from a lager number** TRUTH TABLE:						
9	Sample Calculations	**2. To**						

I/P BCD DATA				O/P EX-3 DATA			
B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

carry.

0 0 1 1 = Small
1 0 0 1 = lager ⊗ 2's Complement = 0111

ie.

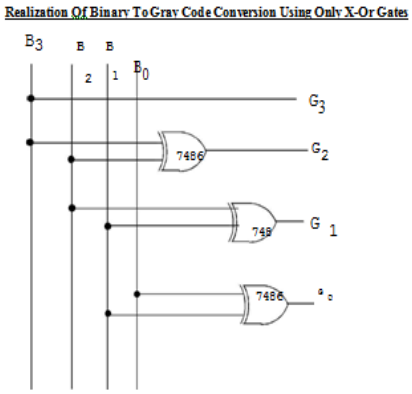
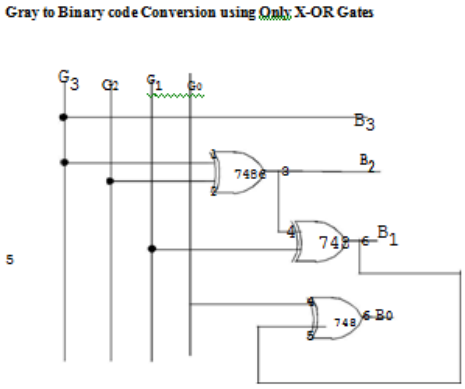
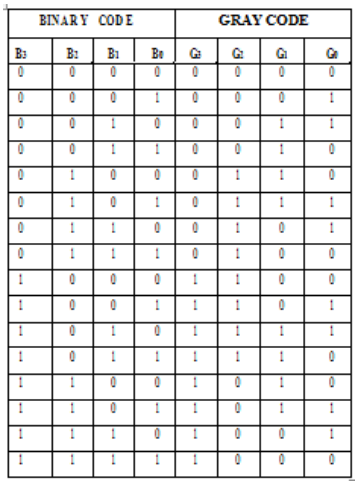
0 0 1 1
0 1 1 1
1 0 1 0

Cout = 0

If the end carry is 0 the result is –ve & is in 2's complement form.

\ S4 S3 S2 S1 = 0 1 1 0 2'S Compliment of 1 0 1 0.

10	Graphs, Outputs	-
11	Results & Analysis	
12	Application Areas	
13	Remarks	
14	Faculty Signature with Date	

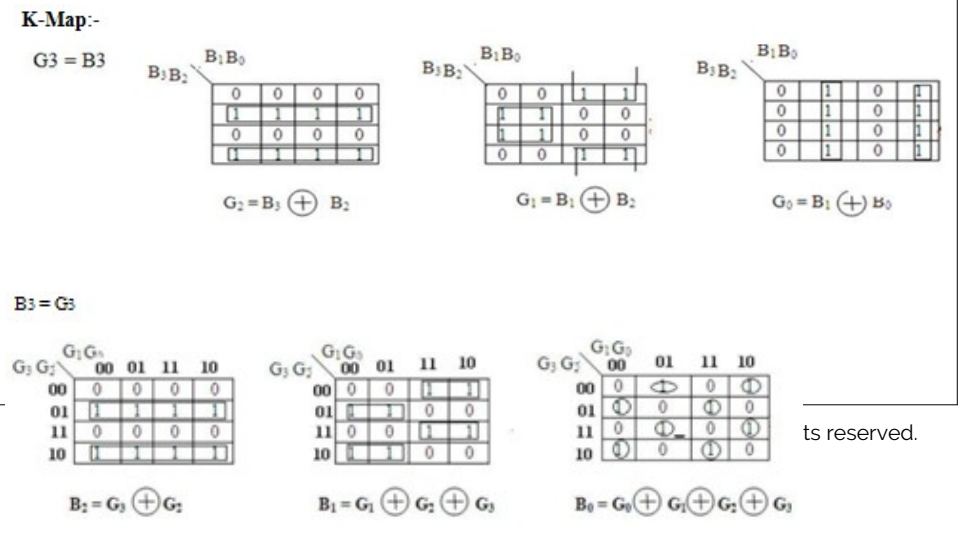
#	Experiment No.:	9	Marks		Date Planned		Date Conducted	
1	Title	REALIZATION OF BINARY TO GRAY CODE CONVERTER AND VICE-VERSA						
2	Course Outcomes	Realize the Binary to Gray code & vice versa using LD trainer kit.						
3	Aim	To Realize Binary To Gray Code Conversion and Vice Versa						
4	Material / Equipment Required	Lab Manual/ Trainer kit, power chord, patch chords, IC's						
5	Theory, Formula, Principle, Concept	$G3 = B3$ $G2 = B3 \oplus B2 = B3\overline{B2} + \overline{B3}B2$ $G1 = B1 \oplus B2 = B2\overline{B1} + \overline{B2}B1$ $G0 = B1 \oplus B0 = B1\overline{B0} + \overline{B1}B0$ $B_2 = G_3 \oplus G_2$ $B_1 = G_1 \oplus G_2 \oplus G_3$ $B_0 = G_0 \oplus G_1 \oplus G_2 \oplus G_3$							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Identify the IC required and Place the IC in the socket of the trainer kit. 2.Make the connections as shown in the circuit diagram. 3.Apply the different combinations of input according to truth table and verify the output.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 							
8	Observation Table, Look-up Table, Output							

BINARY CODE				GRAY CODE			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

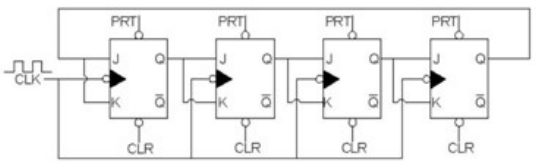
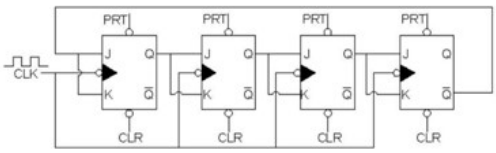
b)DESIGN OF GRAY CODE TO BINARY CODE CONVERTER

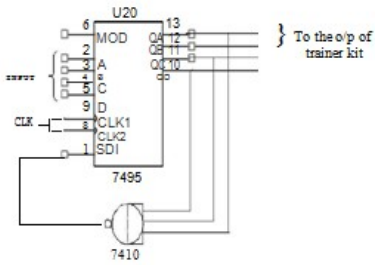
Truth table:

GRAY CODE				BINARY CODE			
G_3	G_2	G_1	G_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

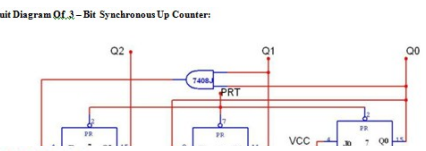
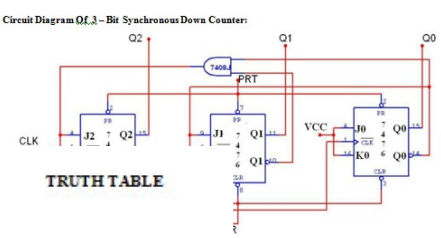
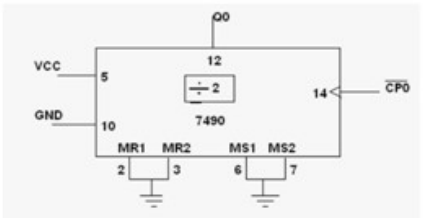
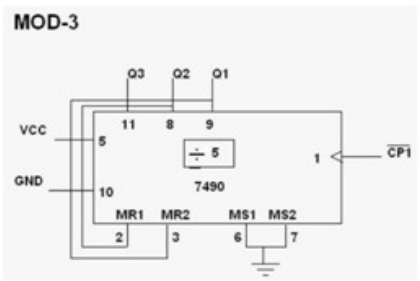
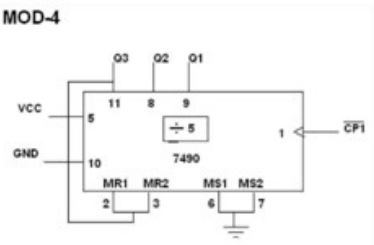
9	Sample Calculations	**K-Map**:- 							

10	Graphs, Outputs	-
11	Results & Analysis	
12	Application Areas	
13	Remarks	
14	Faculty Signature with Date	

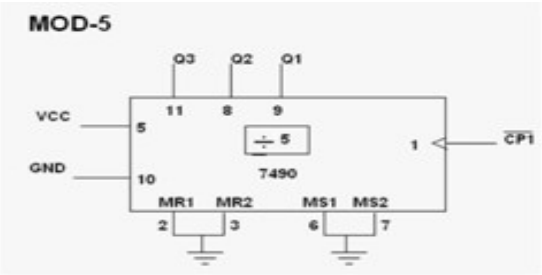
#	Experiment No.:	10	Marks		Date Planned		Date Conducted	
1	Title	DESIGN AND TESTING OF RING COUNTER/JOHNSON COUNTER						
2	Course Outcomes	Design & Realize the Ring & Jogn counter using LD trainer kit.						
3	Aim	To wiring and testing Ring counter/Johnson counter						
4	Material / Equipment Required	Lab Manual/ Trainer kit, power chord, patch chords, IC 7495, 7404.						
5	Theory, Formula, Principle, Concept	A ring counter is a type of counter composed of flip-flops connected into a shift register, with the output of the last flip-flop fed to the input of the first, making a "circular" or "ring" structure. There are two types of ring counters: A straight ring counter, also known as a one-hot counter, connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. A twisted ring counter, also called switch-tail ring counter,walking ring counter, Johnson counter, or Möbius counter, connects the complement of the output of the last shift register to the input of the first register and circulates a stream of ones followed by zeros around the ring. A Johnson counter is a modified ring counter, where the inverted output from the last flip flop is connected to the input to the first. The register cycles through a sequence of bit-patterns. The MOD of the Johnson counter is 2n if n flip-flops are used. The main advantage of the Johnson counter counter is that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1)Connections are made as per the circuit diagram of respective counter. 2)Make the output of any flip-flop high using 3)Disable PRT AND CLR of all flip-flops of counter. 4)Keep applying the clock pulses, verify the truth table of respective counter.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	 						
8	Observation Table, Look-up Table, Output	**Truth table:** CLK Q_A Q_B Q_C Q_D 0 1 0 0 0 1 0 1 0 0 2 0 0 1 0 3 0 0 0 1 4 1 0 0 0 5 0 1 0 0 6 0 0 1 0 7 0 0 0 1			**b)DESIGN OF JOHNSON COUNTER** **Truth Table:** CLK Q_A Q_B Q_C Q_D 0 1 0 0 0 1 1 1 0 0 2 1 1 1 0 3 1 1 1 1 4 0 1 1 1 5 0 0 1 1 6 0 0 0 1 7 0 0 0 0		
9	Sample Calculations	-						
10	Graphs, Outputs	-						
11	Results & Analysis							
12	Application Areas							
13	Remarks							
14	Faculty Signature with Date							

#	Experiment No.:	11	Marks		Date Planned		Date Conducted	
1	Title	DESIGN AND TESTING OF A SEQUENCE GENERATOR						
2	Course Outcomes	Design & Realize the Sequence generator using LD trainer kit.						
3	Aim	Design and testing a Sequence generator for the given sequence ……. 1101011…….						
4	Material / Equipment Required	Lab Manual/ Trainer kit, power chord, patch chords, IC's						
5	Theory, Formula, Principle, Concept	sequence generator is a digital logic circuit whose purpose is to produce a prescribed sequence of outputs. Each output will be one of a number of symbols or of binary or q-ary logic levels. Sequence generators are useful in a wide variety of coding and control applications.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Mode control is made '1' 2.Parallel data (say 0001) is applied to DCBA and a Clock pulse is applied so that $Q_DQ_CQ_BQ_A$=0001 3.Now mode control is made zero and Clock pulse is applied such that 'one' circulates around.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output							
9	Sample Calculations	$D_S = \overline{Q3} + \overline{Q2} + \overline{Q0} = \overline{Q3Q2Q0}$						
10	Graphs, Outputs	-						
11	Results & Analysis							
12	Application Areas	Sequence generators are useful in a wide variety of coding and control applications						
13	Remarks							
14	Faculty Signature with Date							

Q_D	Q_C	Q_B	Q_A	Y=DS
0	1	1	1	1
1	1	1	1	0
1	1	1	0	1
1	1	0	1	0
1	0	1	0	1
0	1	0	1	1
1	0	1	1	1

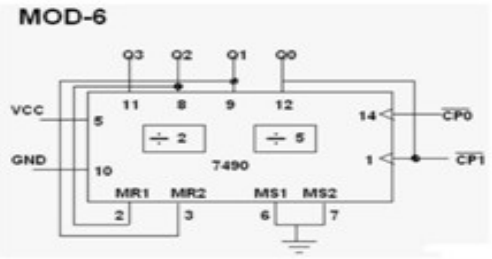
#	Experiment No.:	12	Marks		Date Planned		Date Conducted	
1	Title	REALIZATION OF 3 BIT COUNTERS AS A SEQUENTIAL CIRCUIT USING 7476 AND MOD – N COUNTER DESIGN USING 7490,74192, 74193.						
2	Course Outcomes	Design & Realize the MOD – N Counter Design using LD trainer kit.						
3	Aim	a) To Design and realization of 3-bit Synchronous counter Using7476, b) To Realization of 3-bit Asynchronous Counter Using 7476. c)To Design of MOD-N Counters using IC 7490,74192 / 74193						
4	Material / Equipment Required	IC Trainer Kit, Patch Cords & Ics – 7476,7408, 7490, 74192, 74193						
5	Theory, Formula, Principle, Concept	The number of different output states a counter can produce is called the modulo or modulus of the counter. The Modulus (or MOD-number) of a counter is the total number of unique states it passes through in one complete counting cycle with a mod-n counter being described also as a divide-by-n counter.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	Synchronous Up/Down Counter: 1)Connections are made as shown in the circuit diagram. 2)Switch on the power supply. 3)Clock pulses are applied one by one at the clock I/P and the O/P is observed At Q0,Q1 and Q3. 4)Verify the truth table. Asynchronous Up/Down Counter: 1)Connections are made as shown in the circuit diagram. 2)Switch on the power supply. 3)Verify the truth table. See that it counts from 0 to 7 for Mod-8 counter. MOD-n counters: 1.Connections are made as shown in the circuit diagram. 2.Switch on the power supply. 3.Load the required input at the pre set value pins [P3 P2 P1 P0], this appears at the output when Load is made Low. 4.Then connect Load o/p of the NAND gate. 5.Apply the clock pulses and observe the output as per the Truth Table and Waveforms may be observed						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	Circuit Diagram Of 3 – Bit Synchronous Up Counter:  Circuit Diagram Of 3 – Bit Synchronous Down Counter:  MOD - 2  TRUTH TABLE CLK | Q0 1 | 0 2 | 1 MOD-3  CLK | Q2 | Q1 | Q0 1 | 0 | 0 | 0 2 | 0 | 0 | 1 3 | 0 | 1 | 0 c) Design of MOD-N Counters using IC 7490,74192 / 74193 MOD-4  CLK | Q3 | Q2 | Q1 1 | 0 | 0 | 0 2 | 0 | 0 | 0 3 | 0 | 0 | 1 4 | 0 | 0 | 1						

MOD-5



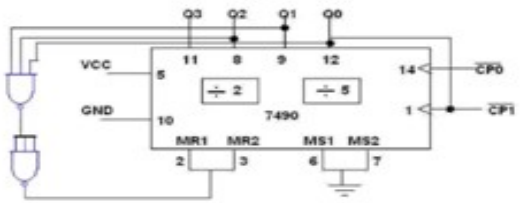
CLK	Q_2	Q_1	Q_0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0

MOD-6



CLK	Q_3	Q_2	Q_1	Q_0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1

MOD-7



CLK	Q_3	Q_2	Q_1	Q_0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0

8	Observation Table, Look-up Table, Output		MOD-8 Synchronous Up Counter

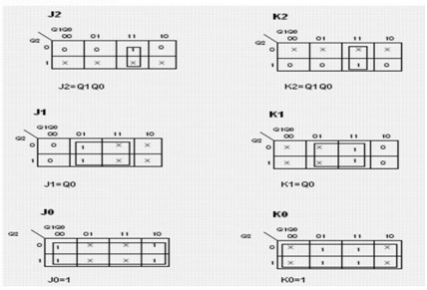
clk	Q_2	Q_1	Q_0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

9	Sample Calculations	MOD-8 Synchronous Up Counter

Excitation Table

Present state			Next State			Flip flop inputs					
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

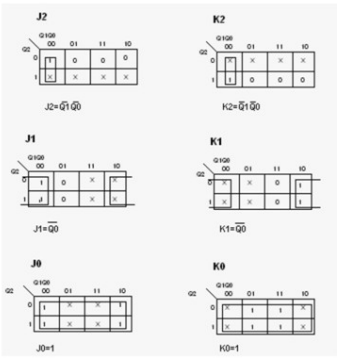
K-MAP of flip flop inputs



MOD-8 Synchronous Down Counter

Excitation Table

Present state			Next State			Flip flop inputs					
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
1	1	1	1	1	0	X	0	X	0	X	1
1	1	0	1	0	1	X	0	X	1	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	0	0	0	1	1	X	1	1	X	1	X
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	0	0	1	1	1	1	X	1	X	1	X



10	Graphs, Outputs	-
11	Results & Analysis	
12	Application Areas	
13	Remarks	
14	Faculty Signature with Date	